Network for Computational Nanotechnology (NCN)

Purdue, Norfolk State, Northwestern, UC Berkeley, Univ. of Illinois, UTEP

Physics-based Nanoelectronic Device Simulations on Petascale Machines

Mathieu Luisier

Overview

- Why Nanoelectronic Device Modeling?
  - From Moore's Law to OMEN
- Application to Nanoscale Device
  - III-V High Electron Mobility Transistors
  - Band-to-Band Tunneling Transistors
- Towards Peta-Scale Device Simulations
  - Simulation Approach
  - Model Implementation
  - Parallelization Scheme
- Conclusion

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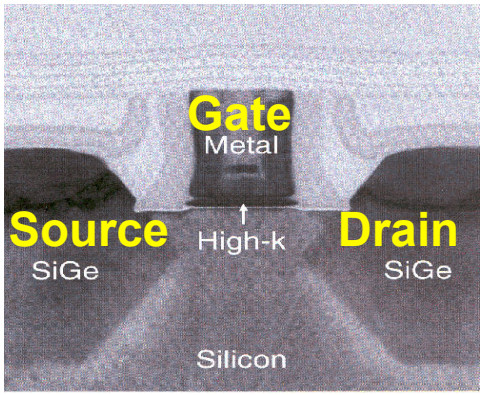
  - **Model Implementation**
  - **Parallelization Scheme**
- **Conclusion**

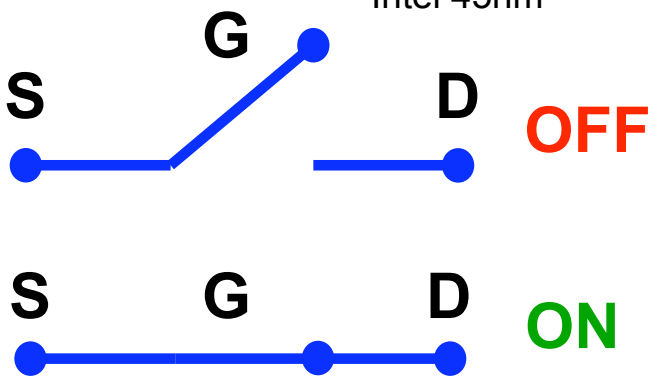
Where do we find them? All around us!

All electronic devices made of transistors:

3-port switch



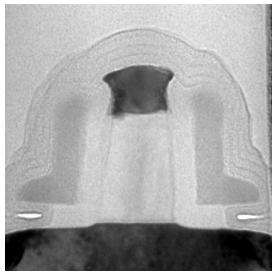
Intel 45nm



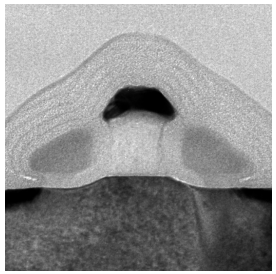
Recent Transistor Evolution

Technical Developments to Enable Moore's Law

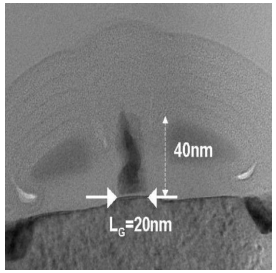
90nm (2003)



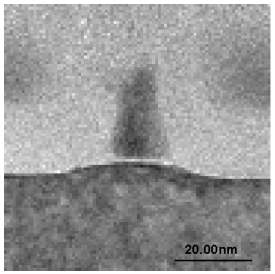
65nm (2005)



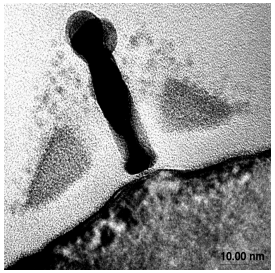
45nm (2007)



32nm (2009)



22nm (2011)



15nm (2013)

??

Source: Intel Corporation

Solution(s) demonstrated till 22nm
40 Years of aggressive Scaling according to Moore's Law
=> Devices at the Atomic Scale

Future of Transistors: Si MOSFET forever?
Heat Dissipation Unmanageable
Quantum Mechanical Effects Dominate
=> New Technical Solutions Required

Search for the Next Generation Switch

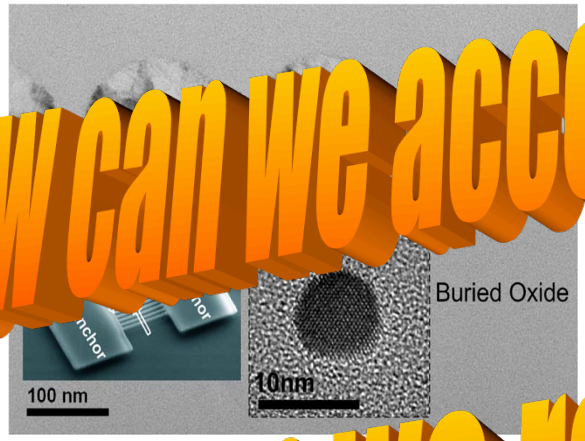
What are the potential solutions?

How can we accelerate innovation?

How can we reduce the cost?

How can we design the best device?

GAA FETs



...bas... a., *Nature Nano.* **3**, 397 (2008)

...raphene ...bon

...MOS...

Y.Q. Wu et al., *EDL* **30**, 700 (2009)

W.Y. Choi et al., *EDL* **28**, 743 (2007)

...ling FETs

What is OMEN?

Multidisciplinary Effort: PHYS - EE - HPC

Device Engineering

- Explore, Understand, Explain, Optimize Novel Designs
- Predict Device Performances
- Predict Eventual Deficiencies Before Fabrication

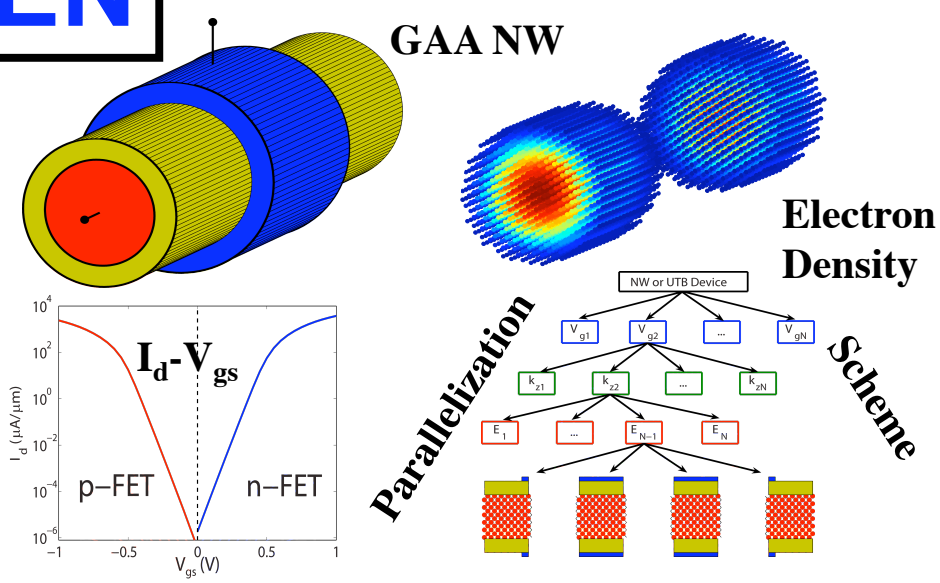
Physical Models

- 3D Quantum Transport Solver
- Accurate Representation of the Semiconductor Properties
- Atomistic Description of Devices
  - Ballistic and Dissipative

OMEN

- Accelerate Simulation Time
- Investigate New Phenomena at the Nanometer Scale
- Move Hero Experiments to a Day-to-Day Basis

Efficient Parallel Computing



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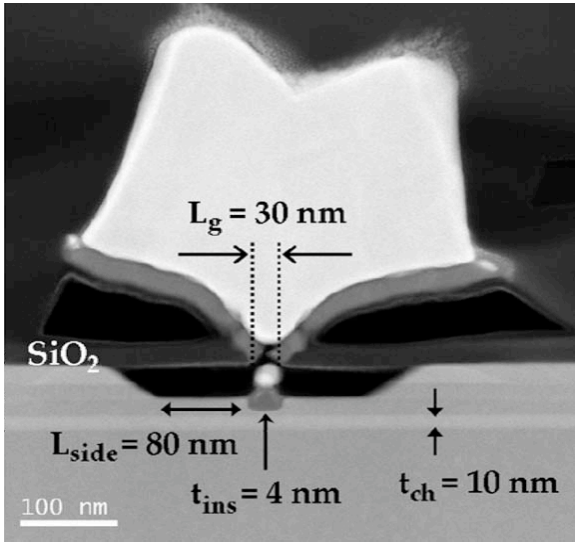
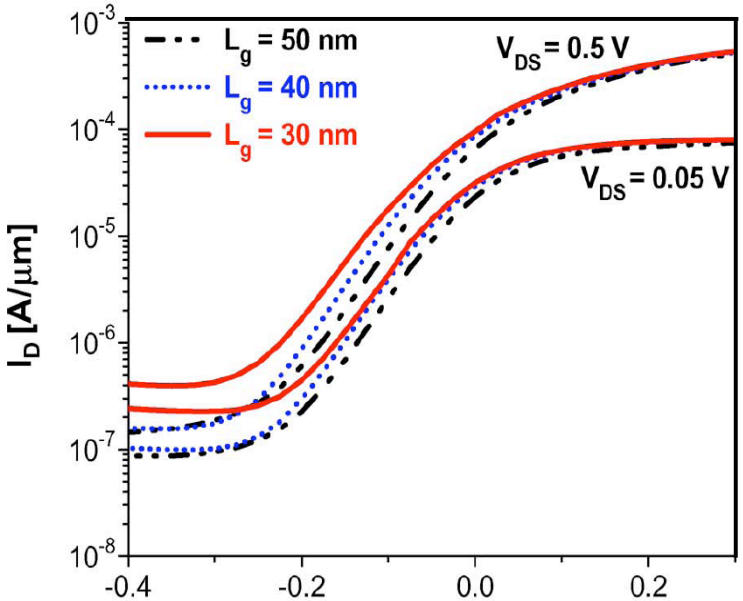
III-V HEMTs: a path towards III-V MOSFETs

Problem: Si material is becoming too slow!
Solution: Materials with higher mobility than Si (InGaAs)

- **III-V HEMTs**: Similar structure to MOSFETs, no high-κ dielectric layer
- For experimentalists: excellent to test performances of III-V channels
- For theorists: excellent to test simulation and physical models



D.H. Kim et al., *EDL* **29**, 830 (2008)



III-V HEMTs: Modeling Challenges

Objective:

- Simulation of III-V HEMTs as first step towards III-V MOSFETs
- Comparison with experimental data
- Design device with scaled L_g

Approach:

- **Multi-scale** domain decomposition
- Strain and material parameter extraction from large atomistic domain
- **Ballistic** transport (no scattering) in the **effective mass** approximation on a reduced domain
- Injection from the Source, Drain, and Gate contacts

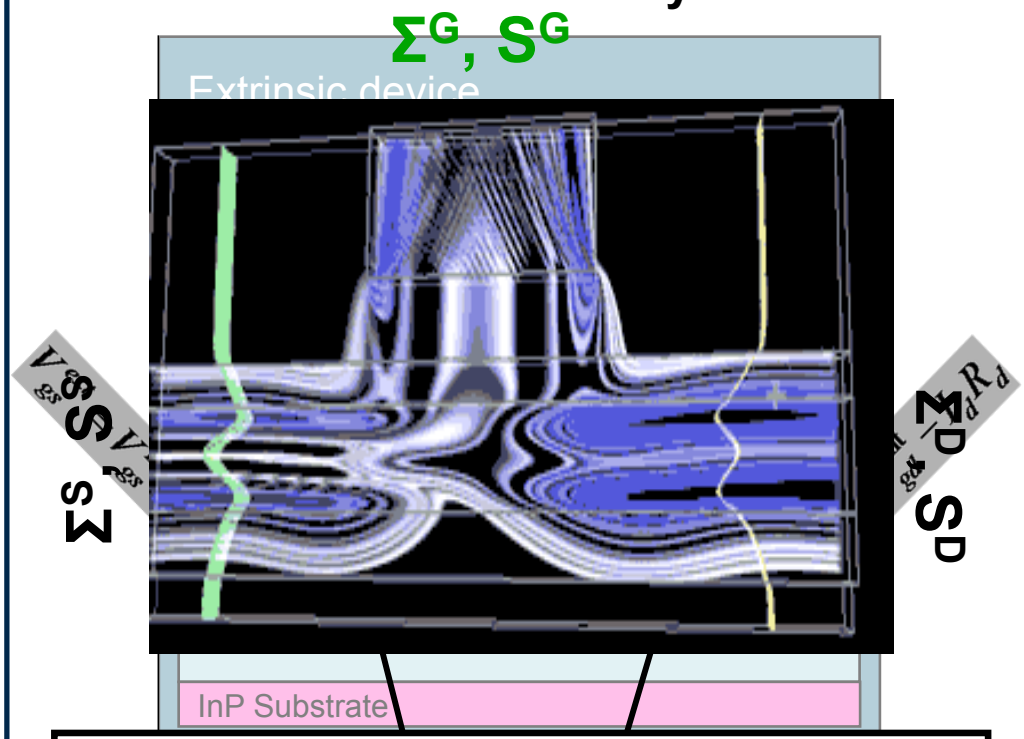
Results/Impact:

- Match experimental results for various gate lengths (30, 40, 50 nm)

Ongoing Work

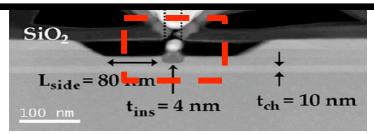
- Better description of S and D contacts

Device Geometry

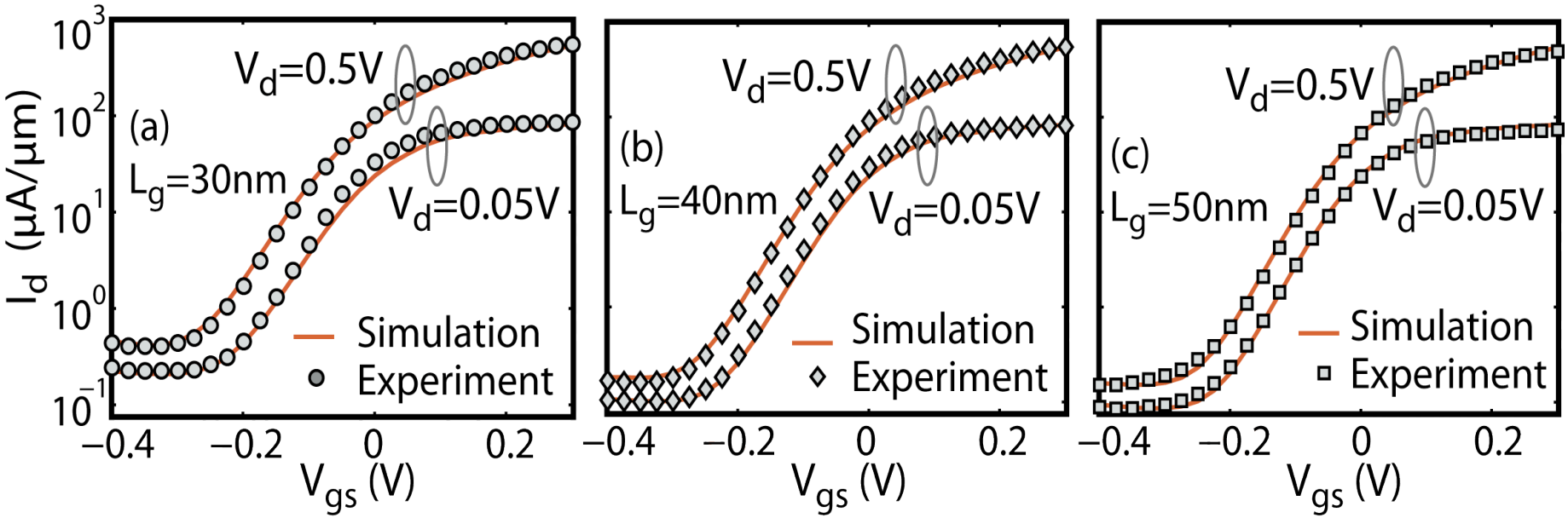


Gate Leakage Modeling

$$(E-H-\Sigma^S-\Sigma^D-\Sigma^G)\cdot C = S^S+S^D+S^G$$



III-V HEMTs: Comparison to Measurement



Important Metrics

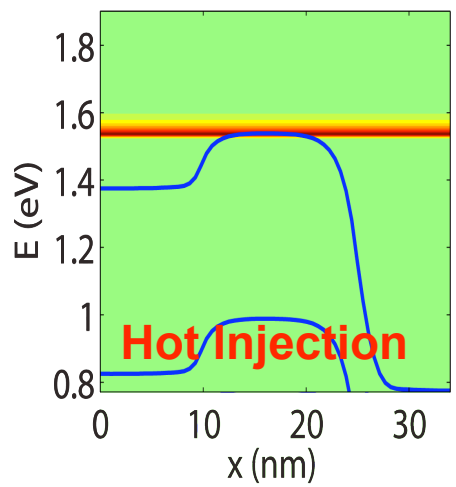
L_g (nm)		S(mV/dec)	DIBL(mV/V)	I_{ON}/I_{OFF}	v_{inj}(cm/s)
30	Exp.	107	169	0.47×10^3	
	Sim.	105	145	0.61×10^3	3×10^7
40	Exp.	91	126	1.38×10^3	
	Sim.	89	99	1.86×10^3	3.11×10^7
50	Exp.	85	97	1.80×10^3	
	Sim.	89	91	1.85×10^3	3.18×10^7

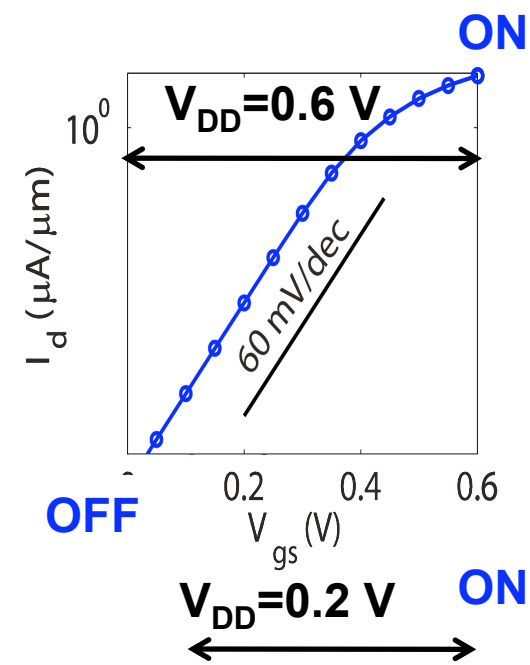
Features:

- **Kraken**: 64-1,024 cores
- Good agreement for all L_g's
- Much higher injection velocities than Si @V_{DD}=0.5 V (3×10^7 for III-V vs 10^7 **for Si**)

Problem: Power Increase

- Subthreshold Swing (SS) limited to 60 mV/dec
- Large I_{ON}/I_{OFF} ratio => large V_{DD}
- High Power Consumption ~V_{DD}^2
- V_{DD} scaling not possible:
  - either increase of I_{OFF}
  - or decreases of I_{ON}





@ low V_{DD}

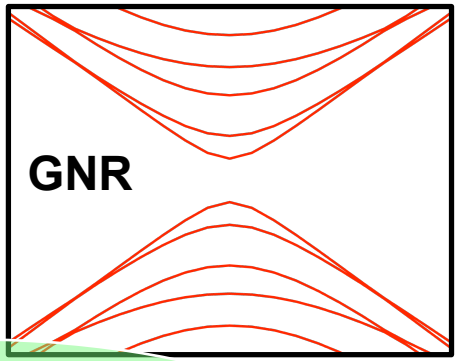
OFF

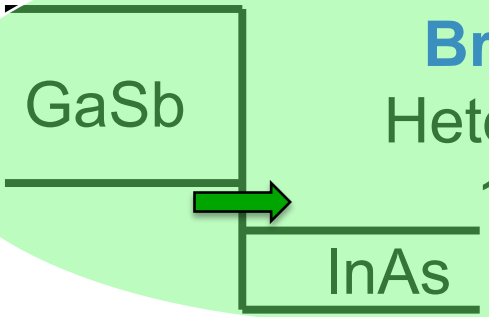
Application to Nanoscale Devices

High Performance TFETs? Low Band Gap Materials!

InSb
E_g=0.169eV
(Bulk)

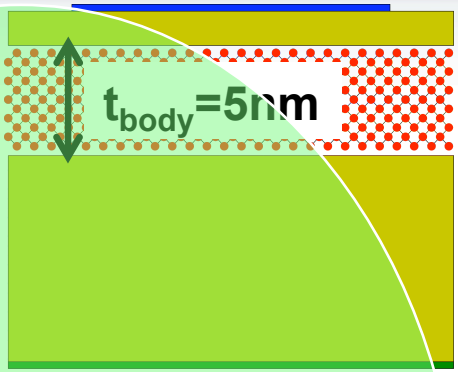
Graphene (C)
Tunable BG
Symmetric BS

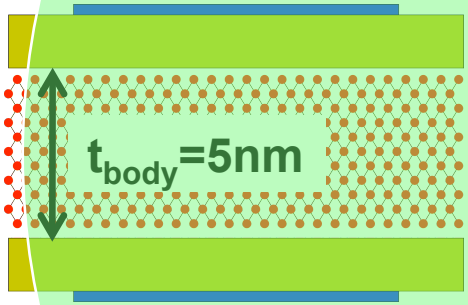




Broken Gap
Heterostructure
150 meV

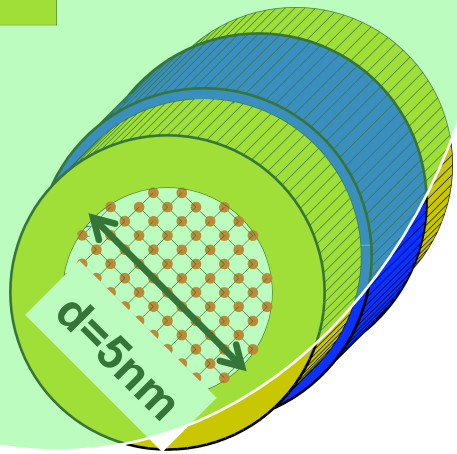
Single-Gate





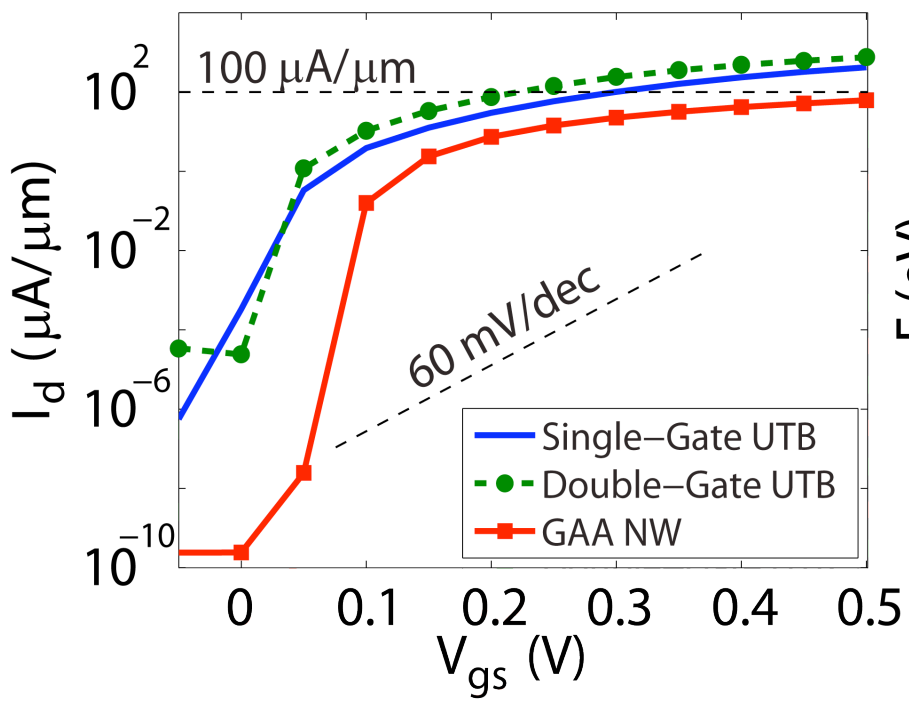
Double-Gate

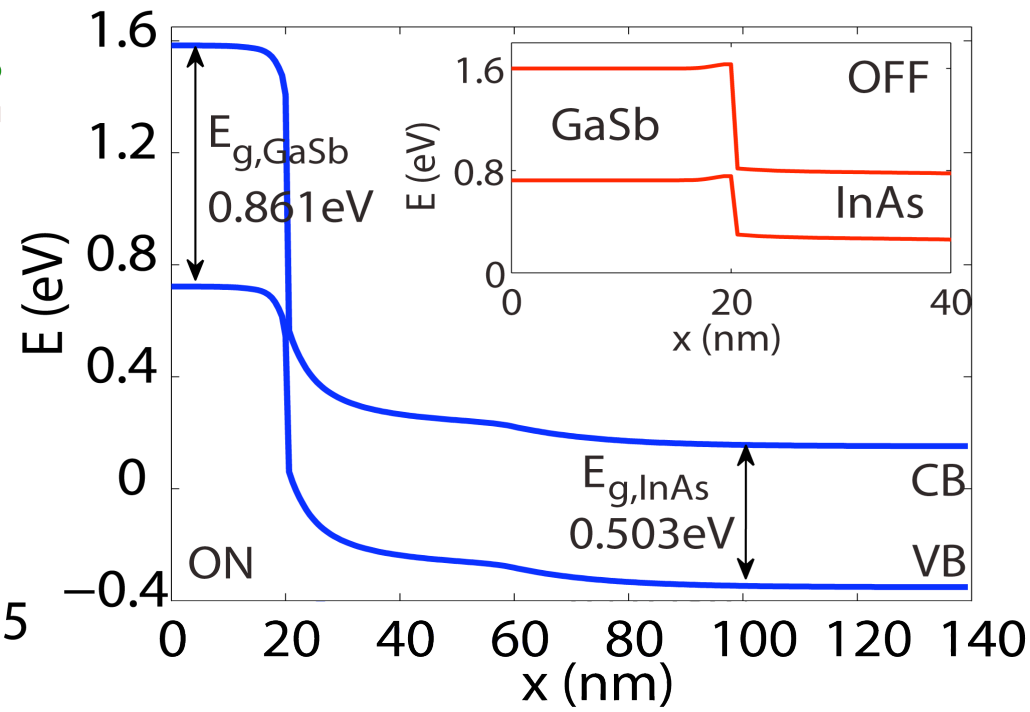
Gate-All-Around



TFETs: Broken-Gap Heterostructure Devices

- Maximum Current of **900 μA/μm** for DG UTB @ **V_{DD}=0.5 V**
- **SS below 60 mV/dec**: GAA (7) < DG (11) < SG (17)
- Simulations on **Kraken** and **Jaguar**: 1,024-20,000 cores





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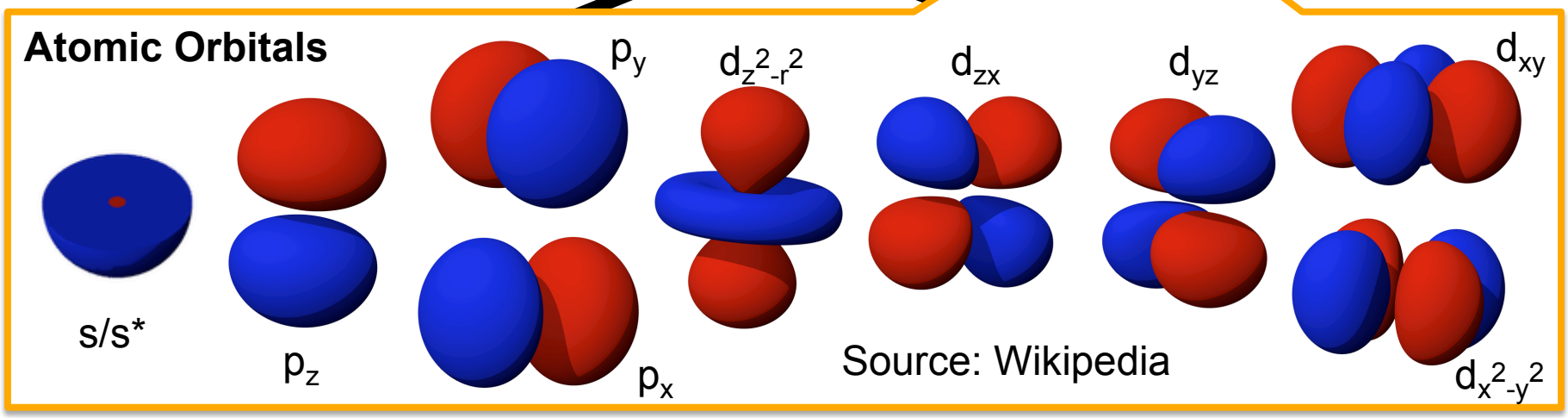
Simulation Approach: Basic Device Equations

Steady-State 1D/2D/3D Schrödinger Equation

$$\mathbf{H} \mid \boldsymbol{\psi}_E > \;=\; E \mid \boldsymbol{\psi}_E >$$

Tight-Binding Ansatz for the Wave Function

$$< \mathbf{r} \mid \boldsymbol{\psi}_E > \;=\; \sum_{\sigma, ijk, \boldsymbol{k}_t} C_{ij}^{\sigma}(E, k_t)\, \Phi_{\sigma}(\mathbf{r} - \mathbf{R}_{ijk})\, e^{i k_t \cdot r_t}$$



What is the originality of the approach?

Atomistic Schrödinger Equation with Open Boundary Conditions

Ballistic Transport, N_A atoms per unit cell, t_b orbitals

"Golden" Standard

1. Open Boundary Conditions

(a) Iterative Methods (Sancho-Rubio)

$$(E - H - t_{10} \cdot g^R \cdot t_{01}) \cdot g^R = I$$

$N_{BC} = N_A \bullet t_B$

(b) Generalized Eigenvalue Problem

$$A \bullet \Phi = \exp(i \bullet k \bullet \Delta) \bullet B \bullet \Phi$$

$N_{BC} = 2 \bullet N_A \bullet t_B$

2. Schrödinger Equation (Matrix G^R)

$$(E-H-\Sigma^B) \cdot G^R = I$$

Recursive Green's Function (RGF)

New Approach in OMEN

1. Open Boundary Conditions

Normal Eigenvalue Problem

$$M \bullet \Phi = 1/(\exp(i \bullet k \bullet \Delta)-1) \bullet \Phi$$

$N_{BC} \leq N_A \bullet t_B$

Reduced Size Problem

Gain Factor: 10-100 in 3-D

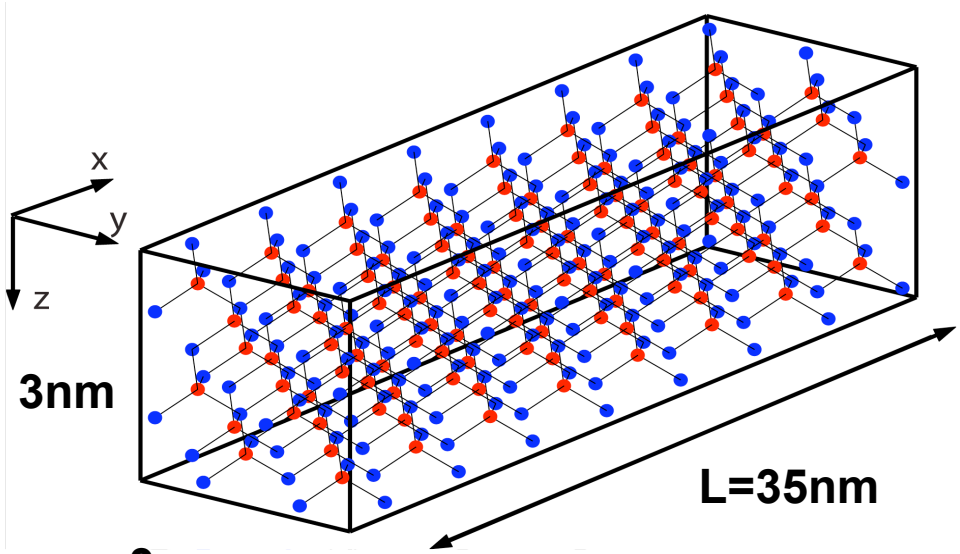
2. Schrödinger Equation (Vector C)

$$(E-H-\Sigma^B) \cdot C = S$$

Sparse Linear Systems of Equations

No Restrictions on the form of (E-H-Σ)

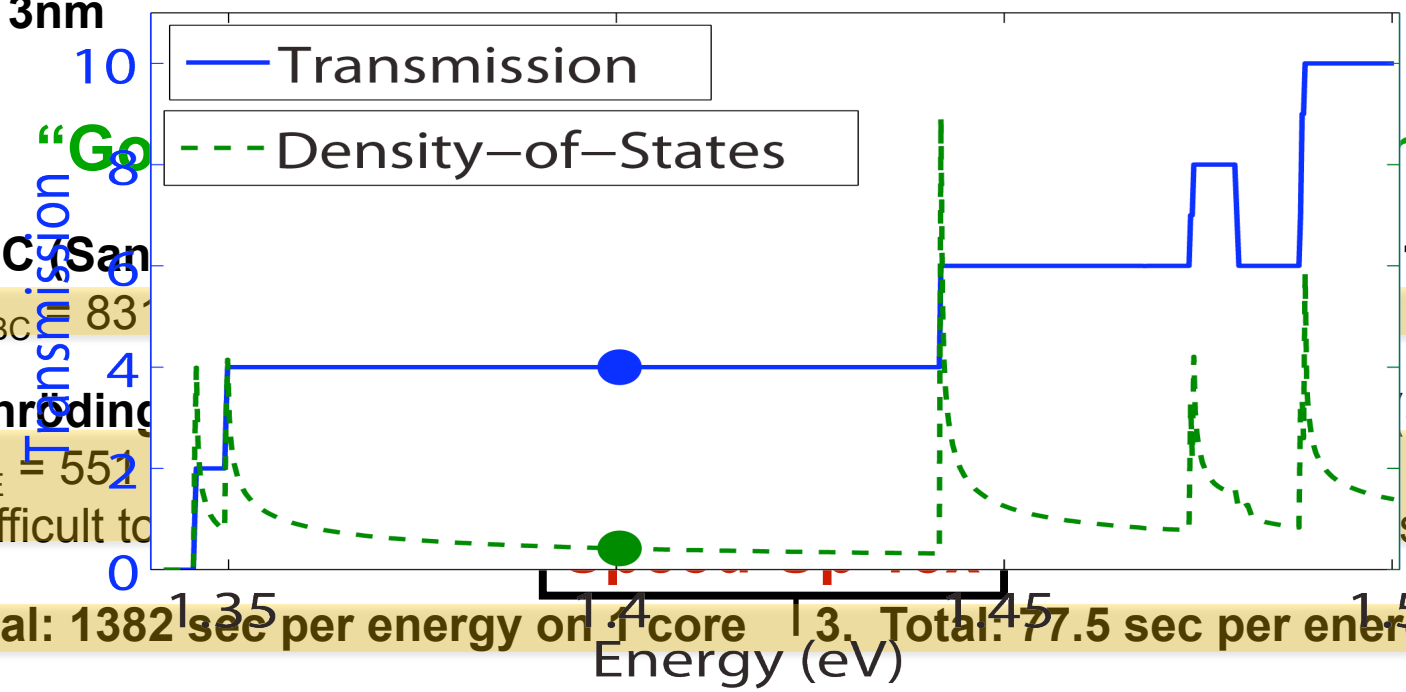
Towards Peta-Scale Device Simulations



Example: 3-D Si Nanowire

N_A = 265 atoms per wire unit cell
N_{UC} = 64 unit cells
N =16,960 atoms in the nanowire

$sp^3d^5s^*$ tight-binding model (t_b=10)
typically: 1,000-1,500 energies



"Go OMEN

1. OBC (San 1330)
   t_{OBC} = 831
2. Schrödinger (Sparse LSE)
   t_{SE} = 551 1 core
   Difficult to s (5.6x faster)
3. Total: 1382 sec per energy on 1 core 3. Total: 77.5 sec per energy on 1 core

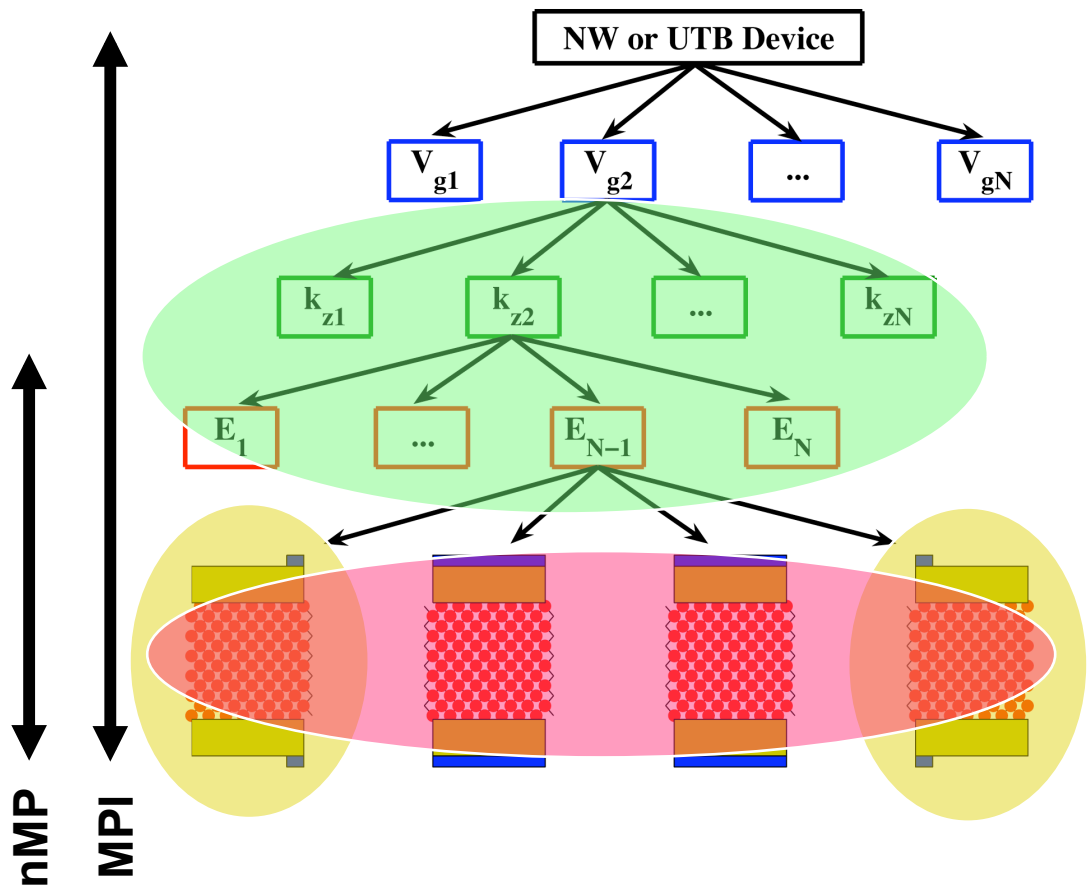
OMEN Parallel Architecture

Objective:

- NEGF with Atomistic Basis

Approach:

- Multi-Level parallelism
  - Voltage
  - Momentum
  - Energy
  - Space
- Mixed MPI / OpenMP
- Dynamic load balancing in double integral
- Computational Interleaving
- Leverage of existing linear solvers (Pardiso, MUMPs, SuperLU, Umfpack, …)
- Novel:
  - Development of new solvers (Optimized Renormalization Algorithm)



Quad-Level Parallelisation Scheme

Tested on multiple platforms

Towards Peta-Scale Device Simulations

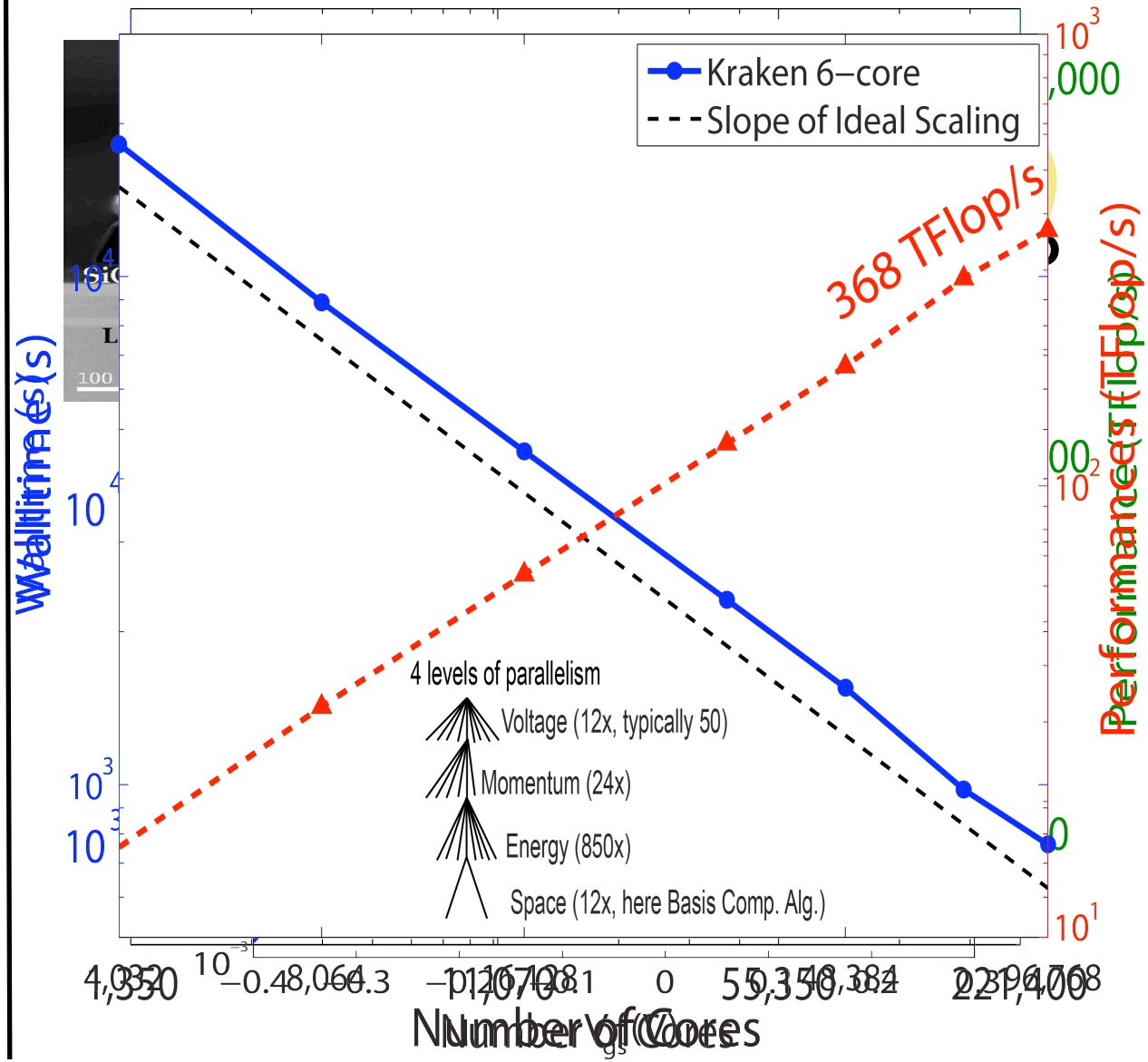
OMEN Scaling to 221,400 Cores

Result:

- Highly efficient parallel algorithm, stressing the most advanced resources available today
- Implementation and test of advanced physics

Impact:

- Move from nano-science to nanodevice engineering in minutes
- Unprecedented insight into atomistic device simulation
- **One of the few codes capable of running on Jaguar full capability**
- Performances at the peta-scale without any external advice or tuning



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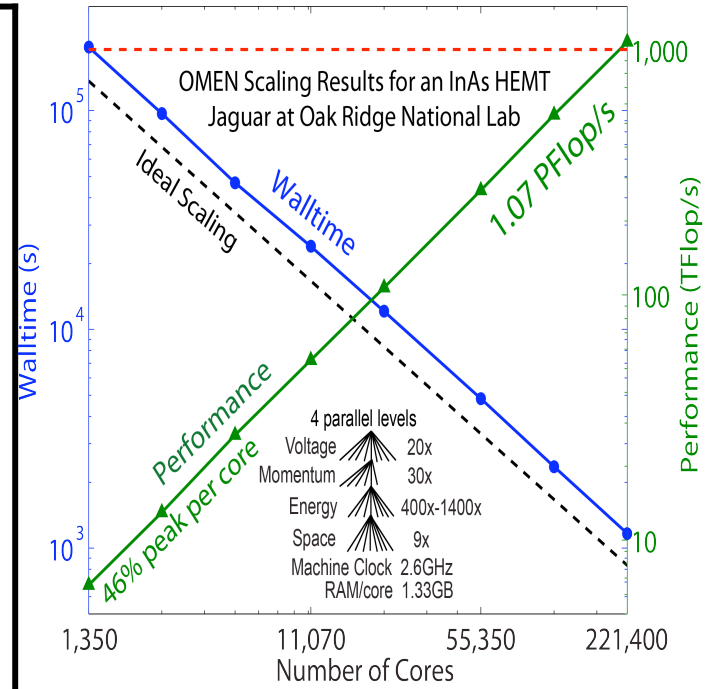
- **Physics-based CAD** HP
  C+PHYS to serve Device Engineering
- **OMEN Simulation Approach**
  3D, full-band, atomistic, quantum transport
  Dedicated to UTB, NW, or HEMT structures
  Sustained Performance > 1 PFlop/s
  Accelerate the technology innovation
- **Outlook and Challenges**
  Close collaboration with experimentalists
  New model development (heat transport)